IN THE CLAIMS:

Please cancel claims 2, 10 and 14 without prejudice or disclaimer, amend claims 1, 3, 7-9, 12 and 15-19, withdraw claims 20-22, and add new claims 23-25 as follows:

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1. (Currently Amended) A level conversion circuit comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having [[a]] said second signal amplitude [[greater than said first signal amplitude]] and being in [[the]] a phase reverse to said first signal; and

a second circuit including a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor [[and]], a second n-channel type MOS transistor and, a third output terminal, a source of said first p-channel type MOS transistor being coupled to a first voltage terminal, a drain of said first p-channel type MOS transistor being coupled to a source of said second p-channel type MOS transistor, a drain of said second p-channel type MOS transistor and a drain of said first n-channel type MOS transistor being coupled to said third output terminal, a source of said first n-channel type MOS transistor being coupled to a drain of said second n-channel type MOS transistor and a source of said second n-channel type MOS transistor being coupled to a second voltage terminal [[whose source-drain routes are connected in series between a first voltage terminal and a second voltage terminal, and the drain of said first p-channel type MOS transistor and the drain of said n-channel type MOS transistor are connected to a third output terminal]],

wherein said second circuit is configured to form[[s]] a fourth signal outputted from said third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis of the signal variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit[[,]] whichever [[is]] signal level changes faster [[in signal level change]] to very a logical threshold of said second circuit so as to accelerate the variation of said fourth signal[[, and supplying said fourth signal from said third output terminal]].

2. (Cancelled)

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3. (Currently Amended) A level conversion circuit according to Claim 1, wherein a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied to the source or drain terminal of the MOS transistor is defined to be one stage, [[the]] a number of [[circuit]] MOS transistor stages gone via by [[which]] a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said [[second]] first output terminal [[goes through and the]] is equal to a number of [[circuit]] MOS transistor stages gone via by [[which]] a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second [[third]] output terminal [[goes through are equal]],

wherein a stage of said MOS transistor stages is defined as a gate-drain path or a gate-source path of a MOS transistor in the level conversion circuit.

4. (Original) A level conversion circuit according to Claim 1, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with change in said second signal or third signal supplied from said first circuit.

5. (Previously presented) A level conversion circuit according to Claim 1, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

6. (Previously presented) A level conversion circuit according to Claim 1, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

7. (Currently Amended) A level conversion circuit according to Claim 1, wherein said first circuit comprises:

a first inverter for logically inverting said first signal [[is further provided, said first circuit having]];

a [[second input terminal]] first node for receiving the output signal of said first inverter; [[and being comprised of]]

a third n-channel type MOS transistor; [[and]]

a fourth n-channel type MOS transistor whose gate terminals are connected respectively to said first input terminal and [[second input terminal,]] said first node;

a third p-channel type MOS transistor whose source-drain path is connected in series to said third n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said fourth n-channel type MOS transistor; [[,]] and

a fourth p-channel type MOS transistor whose source-drain path is connected in series to said fourth n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said third n-channel type MOS transistor, said first output terminal being connected to the drain terminal said fourth n-channel type MOS transistor, said second output terminal being connected to the drain terminal of said third n-channel type MOS transistor, and

wherein said second circuit comprises a second inverter for logically inverting said [[second]] third signal being connected to said [[first]] second output terminal.

8. (Currently Amended) A level conversion circuit according to Claim 7, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with changes in said second signal or the output signal of said second inverter, whichever [[is]] signal level changes faster [[in signal variation]].

9. (Currently Amended) A level conversion circuit according to Claim 8, wherein said second circuit further [[comprising]] comprises a third inverter to control said first p-channel type MOS transistor and second n-channel type MOS transistor according to the second signal supplied from said first output terminal of said first circuit or the output signal of said second inverter, whichever is slower in signal variation.

10. (Cancelled)

11. (Original) A level conversion circuit, according to Claim 1, wherein the state of said first p-channel type MOS transistor or second n-channel type MOS transistor in said second circuit varies in response to a variation of said second signal or third signal supplied from said first circuit, whichever is faster.

12. (Currently Amended) A level conversion circuit comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having [[a]] said second signal amplitude [[greater than said first signal amplitude]] and being in [[the]] a phase reverse to said first signal; and

a second circuit configured to form [[for forming]] a fourth signal outputted from said third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever [[is]] signal level changes faster [[in signal level change]] to very a logical threshold of said second circuit so as to accelerate the variation of said fourth signal, [[and supplying said fourth signal from said third output terminal,]]

wherein said second circuit receives said second signal or third signal supplied from said first circuit and a signal in the reverse phase thereto[[, and the logical threshold is varied so as to accelerate the variation of said fourth signal according to the direction of signal variation]].

13. (Original) A level conversion circuit according to Claim 12, wherein said second circuit has a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor and a second n-channel type MOS transistor whose source-drain paths are connected in series between a first voltage terminal and a second voltage terminal, the drain of said first p-channel type MOS transistor and the drain of said first n-channel type MOS transistor are connected to said third output terminal, high resistance elements are connected respectively in parallel to said second p-channel type MOS transistor and said first n-channel type

MOS transistor, and a delay means is provided to delay said second signal supplied from said first output terminal of said first circuit or said third signal supplied from said second output terminal of said first circuit to control said second p-channel type MOS transistor and first n-channel type MOS transistor or said first p-channel type MOS transistor and the second n-channel type MOS transistor.

14. (Cancelled)

15 (Currently Amended) A level conversion circuit comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having [[a]] said second signal amplitude [[greater than said first signal amplitude]] and being in [[the]] a phase reverse to said first signal; and

a second circuit configured to form [[for forming]] a fourth signal outputted from a third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit[[,]] whichever [[is]] signal level changes faster [[in signal level change, and supplying said fourth signal from said third output terminal]],

wherein [[a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied from the source or drain terminal of the MOS transistor being defined to be one stage, the]] a number of [[circuit]] MOS transistor stages gone via by [[which]] a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said [[second]] first output terminal [[goes through and the]] is equal to a number of [[circuit]] MOS transistor stages gone via by [[which]] a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second [[third]] output terminal [[goes through are]] as three [[each]],

wherein a stage of said MOS transistor stages is defined as a gate-drain path or a gate-source path of a MOS transistor in the level conversion circuit.

16. (Currently Amended) A level conversion circuit according to Claim 1 [[to 15]], wherein [[signals are transmitted in a first amplitude in internal circuits and signals are transmitted and received to and from other external devices in a second amplitude greater than said first amplitude,]] said level conversion circuit [[being]] is included in an input circuit or an output circuit of a semiconductor integrated circuit, and said input or output circuit [[being]] is connected to an external terminal at which signals of said second amplitude are supplied.

17. (Currently Amended) A level conversion circuit according to Claim 16, [[further comprising, in]] wherein said input or output circuit connected to said external terminal [[to which the signals of said second amplitude are inputted,]] includes an inverse level conversion circuit for converting signals of said second amplitude into signals of said first amplitude.

18. (Currently Amended) A semiconductor integrated circuit comprising first and second level conversion circuits, each of which comprising:

[[a first level conversion circuit provided with]] a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and second output terminal for supplying a third signal having [[a]] said second signal amplitude [[greater than said first signal amplitude]] and being in [[the]] a phase reverse to said first signal; and

a second circuit configured to form [[for forming]] a fourth signal outputted from said third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever [[is]] signal level changes faster [[in signal level change]] to very a logical threshold of said second circuit so as to accelerate the variation of said fourth signal, [[and supplying said fourth signal from said third output terminal; and

a second level conversion circuit comprised of a circuit of the same form as said first circuit]].

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19. (Currently Amended) A semiconductor integrated circuit according to Claim 18, wherein said first level conversion circuit is provided on [[the]] a path of transmitting usual operational signals, and said second level conversion circuit[[,]] is provided on [[the]] a path of transmitting testing signals.

20. (Withdrawn) A level conversion circuit according to Claim 4, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

21. (Withdrawn) A level conversion circuit according to Claim 5, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

22. (Withdrawn) A level conversion circuit according to Claim 20, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

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23. (New) A level conversion circuit according to Claim 1, wherein the logical threshold of said second circuit is determined by relative gate widths or relative gate width/gate length ratios of MOS transistors in said first and second circuits.

24. (New) A level conversion circuit according to Claim 12, wherein the logical threshold of said second circuit is determined by relative gate widths or relative gate width/gate length ratios of MOS transistors in said first and second circuits.

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25. (New) A semiconductor integrated circuit according to Claim 18, wherein the logical threshold of said second circuit is determined by relative gate widths or relative gate width/gate length ratios of MOS transistors in said first and second circuits.

IN THE DRAWINGS:

Please enter the attached corrected drawing Fig. 10, in which a legend of "Prior Art" is being added, to replace Fig. 10 as originally filed. A Letter to Draftsperson is also submitted herewith.